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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,266	DENG, XIAOWEI	
	Examiner	Art Unit	
	Son L. Mai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21-23 and 25* is/are rejected.

7)☒ Claim(s) *20 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08-27-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 08-27-03 has been considered.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

As to claim 7, the specification fails to describe "connect bit lines of the memory array to the suspend voltage regulator".

As to claim 8, the voltage range of 0.3 to 0.8 volts does not have sufficient basis in the specification.

As to claim 10, the specification fails to describe "the normal mode voltage is about 1.3 to 1.0 volts and the sourcing suspend voltage is about 0.7 to 0.4 volts below the normal mode voltage".

As to claim 14, the specification fails to describe "the sinking suspend voltage regulator is a low-dropout voltage regulator".

As to claim 20, the specification fails to describe "generating the sinking suspend voltage by a low-dropout voltage regulator."

As to claim 21, the specification fails to describe, "sinking a remaining portion of the generated leakage current". It is noted that figure 5 shows a path 514 as a component for sinking a remaining portion of the generated leakage current. However which components in figures 2 and 3 perform the sinking function as claimed?

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 1 recites the limitation "the suspend state" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim. It appears the Applicant refers to "the suspend mode" in line 3.

6. Claim 8 recites the limitation "the suspend voltage" in line 1. There is insufficient antecedent basis for this limitation in the claim. It appears the Applicant refers to the sinking suspend voltage in claim 1.

7. Claims 2-15 are rejected because in their dependency they include the limitation of the rejected base claim 1.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 5-6, 8, 11-13, 16-19, 21-23 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Tran et al. (U.S. Patent 6,731,564).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Tran et al. discloses a memory device (figure 2) comprising: a memory array (34) comprised of an array of memory cells, wherein the memory array generates leakage current during a suspend mode of operation; a sinking suspend voltage regulator (not shown) that generates a sinking suspend voltage (VBB in figure 3A); a gate-sinking voltage keeper component (78, 146) that controllably connects the memory array to the sinking suspend voltage regulator (at terminal VBB) during the suspend mode and that operates as a leakage current sink; and a controller component (generating signal RETAIN) connected to the gate-sinking voltage keeper component (78, 146) to controllably bias the gate-sinking voltage keeper component, thereby activating the gate-sinking voltage keeper component which in response couples the sinking suspend voltage (VBB) to a portion (WL0) of the memory array upon initiation of the suspend mode.

Regarding claim 5, Tran et al. teaches the gate-sinking voltage keeper component (146) electrically connects to an array supply voltage input (terminal 56, VSB in figure 3C) of the memory array.

Regarding claim 6, Tran et al. teaches the gate-sinking voltage keeper component (78) electrically connects to a word line (WL0) of the memory array.

Regarding claim 8, Tran et al. teaches the sinking suspend voltage (VBB) is from about 0.3 to 0.8 volts (column 4, lines 31-33).

Regarding claim 11, Tran et al. teaches in figure 3C, a footer switch (transistor 160) that controllably connects a VSS voltage (ground node 64) to a VSSA input (VSB) of the memory array.

Regarding claim 12, Tran et al. further teaches in figure 3A, a row periphery circuitry that addresses one or more of the memory cells during normal mode.

Regarding claim 13, Tran et al. teaches the sinking suspend voltage regulator (generating VBB voltage in figure 3C) is further operable as a leakage current sink to dissipate leakage current not sunk by the gate-sinking voltage keeper component (78, 164). (The sinking suspend voltage regulator is connected to a ground node and dissipates leakage current through the ground node.)

Regarding claim 16, Tran et al. discloses a method of operating a memory device in a suspend mode of operation (column 6, lines 7-20) comprising: biasing one or more inputs (node VSB or WL0 in figures 3A, 3C) of a memory array to a sinking suspend voltage (VBB) by one or more gate-sinking voltage keeper components (78, 164); generating leakage current by the memory array (column 1, lines 48-59); and sinking at

least a portion of generated leakage current from the memory array by the one or more gate-sinking voltage keeper components (transistors 78, 164 sink leakage current to a ground node.)

Regarding claim 17, Tran et al. also teaches biasing one or more inputs (VSB or WL0) comprises selectively coupling the sinking suspend voltage (VBB) to the one or more inputs of the memory array by the one or more gate-sinking voltage keeper components (transistor 78 or 164).

Regarding claim 18, Tran et al. teaches a step of connecting a VSSA input (VSB in figure 3C) of the memory array to the sinking suspend voltage (VBB) via one of the gate-sinking voltage keeper components (transistor 164).

Regarding claim 19, Tran et al. also teaches a step of generating a suspend mode of operation control signal (signal RETAIN) that selectively controls the one or more gate-sinking voltage keeper components (transistors 78, 164).

Regarding claim 21, Tran et al. teaches sinking a remaining portion of the generated leakage current (through VBB voltage generator).

Regarding claim 22, Tran et al. teaches isolating a VSSA input (VSB in figure 3C) from a normal mode array voltage supply (ground node 64 when signal RETAIN is active high in the suspend mode.)

Regarding claim 23, Tran et al. teaches at column 6, lines 7-20 and related figures, a method of operating a memory device comprising: biasing a VSSA input (node 56 in figure 3C) of a memory array to a normal array mode voltage (ground node 64) during normal mode; isolating the VSSA input (node 56) and a word line (WL0) from

a sinking suspend voltage (VBB) by one or more gate-sinking voltage keeper components (transistors 78, 164 in figures 3A, 3C) during the normal mode; initiating a suspend mode of operation; isolating the VSSA input (node 56) of the memory array from the normal array mode voltage during the suspend mode of operation; biasing the VSSA input (node 56) to the sinking suspend voltage (VBB) during the suspend mode of operation; biasing the word line (WL0) to the sinking suspend voltage (VBB) during the suspend mode of operation, generating leakage current by the memory array during the suspend mode of operation (column 1, lines 48-59); and sinking at least a portion of the generated leakage current by one or more gate-sinking voltage keeper components (via transistors 78 or 164).

Regarding claim 25, Tran et al. also teaches the VSSA input (node 56) is biased to the sinking suspend voltage (VBB) by one of the gate-sinking voltage keeper components (transistor 164).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being obvious over Tran et al. (U.S. Patent 6,731,564) in view of Houston (U.S. Patent 5,615,162).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art

only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Tran et al. discloses a memory device comprising all of the elements claimed in claim 1. Tran et al. also discloses the gate of the gate-sinking voltage keeper component (78 or 164) being connected to a control signal (signal RETAIN) and the control signal is asserted during the suspend mode of operation (column 6, lines 7-20) as in claims 3 and 4. Tran et al. is silent about the gate-sinking voltage keeper component (transistors 78, 164) comprising a PMOS transistor as in claim 2. In Tran et al., the gate-sinking voltage keeper component (transistors 78, 164) is an NMOS transistor. Either one of the PMOS and NMOS transistors functions as a switch

component for isolating or connecting source and drain terminals. Turning to the Houston reference, at column 4, lines 34-36, the PMOS and NMOS transistor can be used as switches. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a PMOS transistor in place of an NMOS transistor as disclosed in Tran et al., because either one of them can function as a switch to connect or isolate components connected to their source and drain terminals.

Allowable Subject Matter

12. Claims 7, 9-10, 14-15, 20 and 24 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the limitation of a VDDA input of the memory array is biased to a normal mode voltage during a normal mode and to a sourcing suspend voltage during the suspend mode of operation.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yamauchi (U.S. Patent 5715191); Mizuno (U.S. Patent 5726562); Akamatsu (U.S. Patent 5734604); Morishima (U.S. Patent 5969995); and Yamaoka (U.S. Patent 6657911) teach power saving circuits and methods in semiconductor memory devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

03-24-05

Son L. Mai
Primary Examiner
Art Unit 2827